AF/2611
ZFW

TRANSMITTAL OF APPEAL BRIEF (Large Entity)	Docket No. ITL.0513US

In Re Application Of: **Luke A. Johnson**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
09/752,125	December 29, 2000	Khai Tran	21906	2611	8725

Invention: **High-Speed Serial Data Recovery**

COMMISSIONER FOR PATENTS:

Transmitted herewith is the Appeal Brief in this application, with respect to the Notice of Appeal filed on:
October 16, 2006

The fee for filing this Appeal Brief is: No fee believed to be due.

☐ A check in the amount of the fee is enclosed.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☒ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. 20-1504. I have enclosed a duplicate copy of this sheet.

☐ Payment by credit card. Form PTO-2038 is attached.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

Signature

Dated: **December 14, 2006**

Timothy N. Trop, Reg. No. 28,994
TROP, PRUNER & HU, P.C.
1616 S. Voss Road, Suite 750
Houston, TX 77057
713/468-8880 [Phone]
713/468-8883 [Fax]

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)] on
December 14, 2006
(Date)

Signature of Person Mailing Correspondence

Nancy Meshkoff

Typed or Printed Name of Person Mailing Correspondence

cc:

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant:	Luke A. Johnson	Art Unit:	2611
Serial No.:	09/752,125	Examiner:	Khai Tran
Filed:	December 29, 2000	Atty Docket:	ITL.0513US (P10388)
For:	High-Speed Serial Data Recovery	Assignee:	Intel Corporation

Mail Stop **Appeal Brief-Patents**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Date of Deposit: December 14, 2006
I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as **first class mail** with sufficient postage on the date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Nancy Meshkoff

TABLE OF CONTENTS

REAL PARTY IN INTEREST

The real party in interest is the assignee Intel Corporation.

RELATED APPEALS AND INTERFERENCES

None.

STATUS OF CLAIMS

Claims 1-3 (Rejected).

Claims 4-9 (Objected To).

Claim 10 (Rejected).

Claims 11-18 (Objected To).

Claims 19-21 (Allowed).

Claims 22-24 (Rejected).

Claims 25-28 (Objected To).

Claims 29-30 (Canceled).

Claims 1-3, 10, and 22-24 are rejected and are the subject of this Appeal Brief.

STATUS OF AMENDMENTS

The amendments submitted on August 3, 2006 and September 13, 2006 have not been entered.

SUMMARY OF CLAIMED SUBJECT MATTER

In the following discussion, the independent claims are read on one of many possible embodiments without limiting the claims:

1. An apparatus, comprising:

a storage device (Figure 1, 57) to store data (specification at page 5, lines 21-24); and

a block (Figure 2, 210) to adjust the position of the data in the storage device to account for a sampling rate of the apparatus being different than a rate of the received data (specification at page 8, lines 18-26).

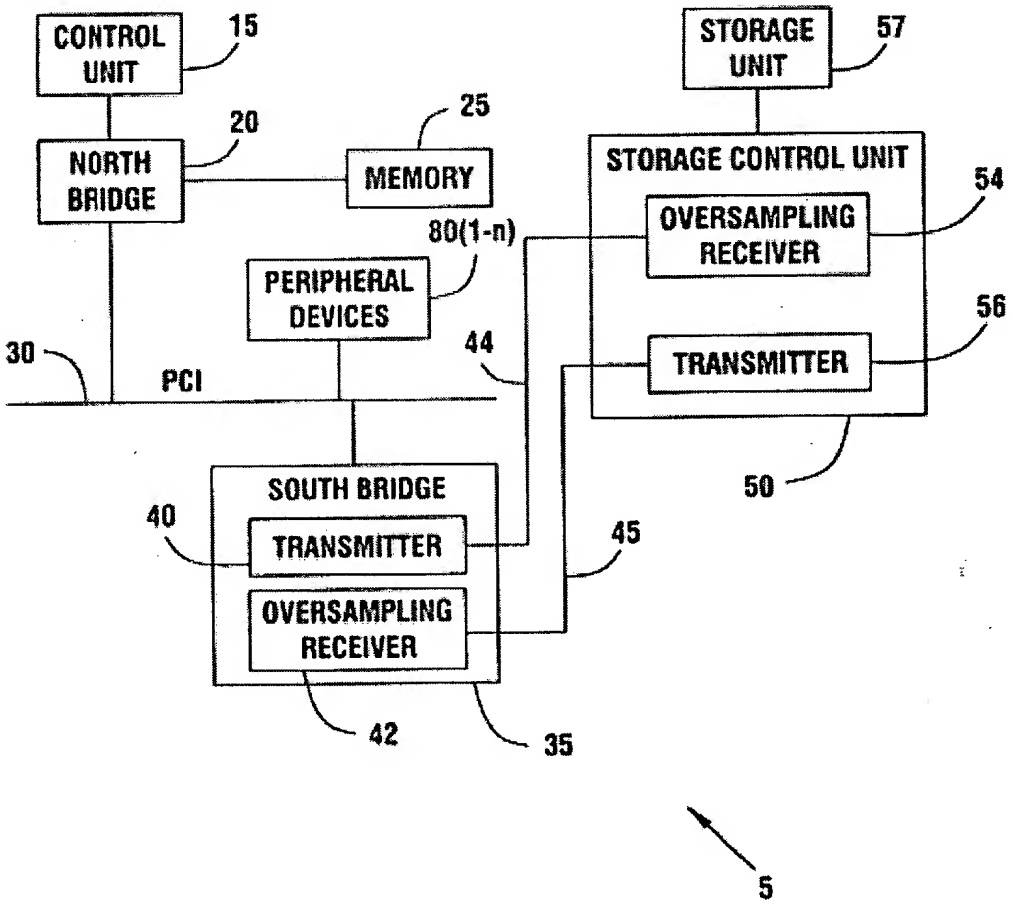

FIG. 1

10. An apparatus, comprising:

a sampling block (Figure 2, 210) to sample incoming data using a plurality of sampling clocks to provide a plurality of samples (specification at page 8, lines 18-26);

a detector block (Figure 2, 225) to detect when the frequency of a sampling clock is different from the rate of the incoming data (specification at page 9, lines 13-22); and

a storage device (Figure 2, 240) to adjust the position of the data in response to detecting the difference in frequency of the sampling clock and the incoming data (specification at page 10, lines 2-12).

22. A method comprising:

storing data in a storage device (specification at page 10, lines 2-12); and

adjusting the location of the data in the storage device to account for a difference in the frequency of the sampling rate versus the data rate of the data being received in the storage (specification at page 8, lines 18-26).

At this point, no issue has been raised that would suggest that the words in the claims have any meaning other than their ordinary meanings. Nothing in this section should be taken as an indication that any claim term has a meaning other than its ordinary meaning.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. **Whether claims 1-3, 10, and 22-24 are anticipated under 35 U.S.C. § 102(e) by Velazquez (US 6, 177,893).**

ARGUMENT

A. Are claims 1-3, 10, and 22-24 anticipated under 35 U.S.C. § 102(e) by Velazquez (US 6, 177,893)?

In the response to arguments in the Final Rejection, two points are made. First, it is pointed out that Velazquez teaches an array. This array is believed to be the converter array 140 since column 8, lines 7-33 are cited under paragraph 3 on page 2 of the office action. However, the array 140 includes M analog-to-digital converters. See column 7, lines 8-11. Thus, the interpretation the Examiner adopts from the Electronic Computer Glossary is clearly inappropriate. Resort to the glossary is improper where the cited reference itself defines what it is he is talking about. What he is talking about is an array of analog-to-digital converters, not a storage. Therefore, for this first reason, reconsideration is requested.

Secondly, it is noted that there is no adjusting of position or data in the alleged storage device because the compensation includes rate changers to adjust the signal rate from the rate used by the converters in the array to the effective sample rate of the full system. Cited in support thereof, again, is column 8, lines 7-33. It is explained in that material that if the individual converters in the array are sampling at 1/M, the effective sample rate of the full system, then digital up samplers can be used to increase the rate by a factor of M. But this is akin to the situation where a series of roller derby rolling vehicles are in a race in a line one after the other. When they come to a hill, they are accelerated, but they are all accelerated by the same hill and, thus, their positions never change, they just simply increase in speed. There is no suggestion in this material that the position of any data element is changed. Doing so would be unusual and no provision is made for how to reassemble the data once positions are changed. Since there is no discussion of changing the positions of the data, it is respectfully submitted that reconsideration would be appropriate.

With respect to the rejection of claim 10, it is reiterated from the prior response that nothing that corresponds to the sampling block or the detector block is cited. Certainly, the rejection is not commensurate with the claims and, therefore, reconsideration is requested. There is no identification of a sampling block or detector block to detect when the frequency of the sampling clock is different from the rate of the incoming data. Nor, as described above, is there any storage device that adjusts the position of the data in response to detecting the difference in

frequency of the sampling clock in the incoming data. This is due, at least initially, because there is no detecting of that difference in frequency and, finally, because there is no storage device that adjusts position.

Applicant respectfully requests that each of the final rejections be reversed and that the claims subject to this Appeal be allowed to issue.

Respectfully submitted,

Date: December 14, 2006

Timothy N. Trop, Reg. No. 28,994
TROP, PRUNER & HU, P.C.
1616 S. Voss Road, Suite 750
Houston, TX 77057
713/468-8880 [Phone]
713/468-8883 [Fax]

Attorneys for Intel Corporation

CLAIMS APPENDIX

The claims on appeal are:

1. An apparatus, comprising:

a storage device to store data; and

a block to adjust the position of the data in the storage device to account for a sampling rate of the apparatus being different than a rate of the received data.

2. The apparatus of claim 1, wherein the block adjusts a portion of the data in response to receiving a plurality of bits in response to sampling a portion of an incoming data.

3. The apparatus of claim 1, wherein the block comprises a detector to detect the at least one sampling error.

10. An apparatus, comprising:

a sampling block to sample incoming data using a plurality of sampling clocks to provide a plurality of samples;

a detector block to detect when the frequency of a sampling clock is different from the rate of the incoming data; and

a storage device to adjust the position of the data in response to detecting the difference in frequency of the sampling clock and the incoming data.

22. A method comprising:

storing data in a storage device; and

adjusting the location of the data in the storage device to account for a difference in the frequency of the sampling rate versus the data rate of the data being received in the storage.

23. The method of claim 22, further comprising sampling incoming data to provide a plurality of samples.

24. The method of claim 23, further comprising detecting at least one sampling error in the plurality of samples.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.